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PATENT APPLICATION
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Schultz et al. **Examiner**: Jasmine Song
Serial No: 10/723,781 **Art Group**: 2188
Filing Date: 11/26/03 **Docket No**: SIG000103
Title: USE OF MULTIPLE OVERLAYS TO IMPORT PROGRAMS FROM EXTERNAL MEMORY

Date: 9/15/06

Pre-Appeal Brief Request for Review

1. In the Final Office Action dated 5/15/06, the Examiner rejected claims 1-19 under 35 USC § 102 (b) as being anticipated by Everett (U.S. Patent No. 6,220,510). Applicant respectfully believes that there is a clear deficiency in the prima facie case in support of these rejections and requests review of the allowability of claims 1-19.

2. Claims 1-19 have been rejected under 35 USC § 102 (b) as being anticipated by Everett (U.S. Patent No. 6,220,510). In the above referenced Final Office Action, the Examiner stated in the Response to Applicant's Arguments that Applicant's arguments do not comply with 37 CFR 1.111(c) because they do not clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the prior art disclosed by the references cited or the objections made. Such a statement is a clear deficiency in support of maintaining the present rejection.

MPEP 2131 states, in part, that "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference."

Accordingly, to overcome an anticipation rejection, the applicant needs to show that the prior art reference does not include each and every element as set forth in the claims. The applicant has done so in the response to the previous office action and repeats the 37 CFR 1.111 (c) compliant below.

Everett teaches at column 4, lines 20-31, that:

> At a general level, each AAM space created for each application being executed includes two separate address spaces, one for the program code itself and one for the program data which is stored and/or used by the application. The program data address space is effectively divided into three segments: a Static segment, a Dynamic segment and a Public segment which are described in more detail in conjunction with FIG. 1. As stated above, the Static, Dynamic and Public segments are logically mapped to the physical memory; they are virtual memory segments as opposed to physical memory segments. [emphasis added]

Everett further teaches at column 4, lines 53-60, that:

> Within the allocated AAM data space 101, the Static portion of the memory is non-volatile which is not erased after power is removed from the IC card (such as EEPROM), the Dynamic space is volatile (such as RAM) which may be erased after power is removed from the card and the Public space is also volatile (such as RAM). [emphasis added]

Everett further teaches at column 5, lines 49-55, that:

> Referring to FIG. 1, the allocated Static segment 103 contains the application's non-volatile data. Static data includes data which is associated with each application for every transaction such as the card user's name, account number, PIN value and address. Static data also includes variable data which is stored for use in future transactions using the application.

Everett further teaches at column 6, lines 8-12, and column 8, lines 21-23, respectively, that:

> The Dynamic segment 107 contains the application's volatile or temporary data. Dynamic data includes data which is temporarily used during the execution of an application such as intermediate values used in calculations or working variables.
>
> The Public segment 105 is used for command and response data being passed between an IFD and an application.

As such Everett teaches that an AAM creates a virtual memory for program data where data that is to be retained beyond execution of a current application is stored in a static section of the virtual memory (e.g., EEPROM) and data that is not to be retained beyond the execution of a current application is stored a dynamic section of the virtual memory or a public section of the virtual memory. Everett, however, does not teach or suggest allocating a first portion of a first memory as a static section to store a main program which uses functional programs stored in a second memory as is claimed in claim 1. Further, Everett does not teach or suggest allocating a second portion of the first

memory as a dynamic section to store other programs, the dynamic section including a plurality of overlay spaces to overlay the functional programs loaded from the second memory to conserve memory capacity of the first memory as is claimed in claim 1.

As such, the applicant contents that claim 1 overcomes the present rejection.

Claim 6 claims a method that includes executing a program statement of a main program to perform a particular functional operation by identifying a corresponding functional program using a resource identifier and by specifying an entry point into one of the overlay spaces; using the resource identifier to identify a corresponding functional program to perform the particular functional operation; loading the functional program into an overlay space specified by the specified entry point; and executing the functional program in the overlay space. [emphasis added]

Everett does not teach or suggest such a method. Everett, however, does teach at column 9, lines 12-34, that:

> FIG. 2 shows an extended illustration of the AAM implemented architecture. Data memory space 201 includes the three segments Static, Public and Dynamic as previously described. Code memory space 203 contains the program instructions for an application stored on the IC card. The application instructions are preferably stored in an executable form which can be interpreted by the resident operating system but can also be stored in machine executable form. Instruction 205 is stored at one location in the code memory space 203. Additional instructions are stored in other locations of memory space 203. Two additional registers 207 and 209 are used in the AAM architecture. A code pointer (CP) register 207 indicates the particular code instruction to be next executed. In the figure, the register indicates, e.g., through an offset or pointer means, that instruction 205 is the next to be executed. Condition Control Register 209 contains eight bits, four of which are for use by the individual application and four of which are set or cleared depending upon the results of the execution of an instruction. These condition codes can be used by conditional instructions such as Branch, Call or Jump. The condition codes can include a carry bit, an overflow bit, a negative bit and a zero bit. [emphasis added]

Everett further teaches at column 6, lines 49-51, and at column 10, lines 6-7, respectively, that:

A delegation function occurs when one application selects another application to process a command instead of processing the command itself.

FIG. 3 shows a flow chart of the steps which are performed when a delegate request is executed.

As such, Everett teaches storing the program instructions for applications in one memory space (e.g., code memory space 203), where one application can delegate a function to be carried out by another application. Everett, however, does not teach loading the functional program into an overlay space specified by the specified entry point; and executing the functional program in the overlay space as is claimed in claim 6. Thus, the applicant believes that claim 6 overcomes the present rejection.

Claim 11 claims an apparatus that includes a first memory and a second memory. The first memory includes a first portion as a static section to store a main program which uses functional programs and a second portion as a dynamic section to store other programs which reside in the first memory for a shorter duration than the main program, the dynamic section including a plurality of overlay spaces to overlay functional programs. The second memory is operably coupled to store the functional programs and to load a functional program specified by a resource identifier in the main program to a corresponding overlay space specified by an entry point specified by the main program. [emphasis added]

The applicant believes that the arguments that distinguished claim 1 over Everett are applicable in distinguishing claim 11 over Everett.

Claim 15 claims a multi-function handheld device that includes a system on a chip integrated circuit and an external memory. The system on a chip integrated circuit includes an internal memory arranged to have a first portion as a static section to store a main program which uses functional programs and a second portion as a dynamic section to store other programs which reside in the internal memory for a shorter duration than the main program, the dynamic section including a plurality of overlay spaces to overlay the functional programs. The external memory is operably coupled to the integrated

circuit to store the functional programs and to load a functional program specified by a resource identifier in the main program to a corresponding overlay space specified by an entry point specified by the main program. [emphasis added]

The applicant believes that the arguments that distinguished claim 1 over Everett are applicable in distinguishing claim 15 over Everett.

Claims 2-5 are dependent upon claim 1, claims 7-10 are dependent upon claim 6, claims 12-14 are dependent upon claim 11, and claims 16-19 are dependent upon claim 15, each of which introduces additional patentable subject matter. The applicant believes that the reasons that distinguish claims 1, 6, 11, and 15 over the present rejection are applicable in distinguishing claims 2-5, 7-10, 12-14, and 16-19 over the same rejection.

RESPECTFULLY SUBMITTED,

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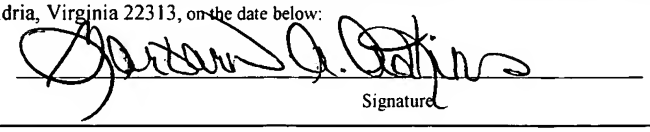
9-15-2006 

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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): SIG000103

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Application Number	Filed
10/723,781	11/26/03

First Named Inventor: Schultz et al.

Art Unit	Examiner
2188	Jasmine Song

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- ☒ attorney or agent of record. Registration number 33,534
- ☐ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34

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9/15/06
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☒ *Total of 1 forms are submitted.